

REMARKS

Claims 1-49 are pending in this application. Claims 37-49 are newly added claims. No new matter has been added. Claims 1, 35, and 36 are the independent claims.

The Examiner rejected Claim 1 under 35 U.S. C. 102(b) as being anticipated by Baratloo et al. Claim 1 (as well as Claims 2-34) was also rejected under 35 U.S.C. 103(a) as being unpatentable over Rosenberry (U.S. Patent 5,349,682) in view of Hagersten et al. (U.S. Patent 5,862,357), Hortensius et al. (U.S. Patent 5,917,629), Chen (U.S. Patent 5,809,190), and Slater ("The Microprocessor Today"). Applicant respectfully disagrees. However, in order to expedite allowance of the claims, Applicant has amended claim 1 to include that the plurality of inner firewalls comprise a hardware component and/or a firmware component (supported by, for example, Applicant's FIGs. 10A and 23A) and that the at least two microprocessors are located on a single microchip (supported by, for example, Applicant's FIGs. 10A, 10C, 16R-16T, 20B, and originally filed Claims 18, 35, and 36).

Baratloo et al. does not disclose the feature of the plurality of inner firewalls comprising a hardware component and/or a firmware component. In contrast, Baratloo et al. discloses "Charlotte", a Web-based virtual machine model that "is implemented solely in Java" (see Baratloo et al., page 1), a software program. As noted by Baratloo et al., "this means that a Charlotte program provides the same level of security and reassurance as a Java program." (See Baratloo et al., page 2.) Since Charlotte is Web-based, the "same level of security and reassurance as a Java program" means that any of the security features of Java are accessible to any programmer with Web access, which could be any programmer in the world. Thus, any or all of the security features of Charlotte could be

defeated by remote access of a programmer to, for example, a memory component. In contrast, Claim 1 provides a personal computer with an inner firewall comprising a hardware component and/or a firmware component. The inner firewall with a hardware component and/or a firmware component denies access to the memory component of the personal computer if attempted by another computer. The use of a hardware component and/or a firmware component, as now claimed by the Applicant in Claim 1, can preclude remote access by any programmer from any network, including the Internet and the Web, from modifying the security features claimed by the applicant, including denying network access to a first memory component in Claim 1.

With respect to Rosenberry, Hagersten et al., Hortensius et al., Chen, or Slater, none of these references teach inner firewalls, which inner firewalls comprise a hardware component and/or a firmware component. In fact, Hagersten et al. actually teaches away from providing a firewall with a hardware component and/or a firmware component because it describes a software program that controls access to local, private memory and global memory. (See Hagersten et al. FIGURE 4.) In contrast to Applicant's Claim 1, "global" memory is not necessarily network accessible, since Hagersten et al. describes a "Hierarchical SMP Computer System," which is essentially a supercomputer in a box or other contained space depending on the configured size, for which no external network system like an Internet or Intranet is described. Far from being a network security feature, the Hagersten et al. invention is a "hierarchical bus architecture [that] eliminates global broadcasts of local transactions" to avoid data congestion from limited bus bandwidth. (See lines 15-22 and 33-35 of Column 2.)

In light of the above comments, Applicants submit that Claim 1 is allowable. Claims 2-34 all include additional, patently distinct elements and unique new combinations that define clearly over the prior art references. The artificial combination of those references lacks any teaching within the references suggesting even part of the combinations and therefore the combinations are simply the product of hindsight of the applicant's invention. Moreover, Claims 1-34 depend on Claim 1 and are thus also allowable. Applicant notes that all amendments are supported by Applicant's application. Claims 2-14, 16, 20-34 have been amended for clarification purposes, and have not added new limitations. Claims 15 and 17-19 have been amended to include additional limitations, and are supported, for example, as follows: Claim 15 (FIGs. 23A-23C); Claim 17 (FIGs. 16Q-16U); Claim 18 (FIGs. 10A, 10C, 16R-16T, 20B, and original Claim 18); and Claim 19 (FIGs. 10P and 10Q).

Claims 35 and 36 were rejected under the judicially created doctrine of obviousness double patenting over claims 1-83 of U.S. Patent 6,167,428 and claims 52-54 of U.S. Patent Application 09/669,730. Enclosed are terminal disclaimers that are submitted to overcome this rejection. The Examiner indicated that Claims 35 and 36 comprised allowable subject matter. Claims 35 and 36 have been amended to clarify the claims, but have not changed substantially. Applicant thus submits that Claims 35 and 36 are allowable. Claims 37-49 all include additional, patently distinct elements and unique new combinations that define clearly over the prior art references. Moreover, new Claims 37-49 depend on Claims 35 and 36, and are thus also allowable for the same reasons. Claims 37-49 are supported, for example, as follows: Claims 37-38 (FIGs. 10A and 23A); Claims 39-40 (FIGs. 10A, 10C, 16R-16T, 20B, and originally filed Claim 18);

Claims 41-42 (FIGs. 16Q-16U); Claims 43-44 (FIGs. 10P and 10Q); Claims 45-47 (FIGs. 10A-10D, 10J-10Q, 16R-16U, 16X-16AA, 17B-17D, 20A-20B, 21A-21B, 22C, and 23A-23C); Claims 48 and 49 (original Claim 6).

Applicant believes the objections and rejections in the Office Action have been addressed and that the application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone should the Examiner believe that personal communication will expedite prosecution of this application.

Respectfully submitted,

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